CLAIMS

What is Claimed is:

1. A semiconductor device having a surface, comprising:

a plurality of conductive sub-surface regions of a first conductivity each formed beneath said surface, wherein said conductive sub-surface regions form a sub-surface structure for routing a body-bias voltage, wherein said sub-surface structure has a perimeter;

an isolation structure formed within said perimeter of said sub-surface structure such that said isolation structure creates a gap in said sub-surface structure; and

at least one metal structure formed above said surface, wherein said metal structure spans said gap and is coupled to said sub-surface structure via a plurality of tap contacts.

2. The semiconductor device as recited in Claim 1 wherein said sub-surface structure is a diagonal sub-surface mesh structure.

3. The semiconductor device as recited in Claim 1 wherein said sub-surface structure is an axial sub-surface mesh structure.

4. The semiconductor device as recited in Claim 1 wherein said sub-surface structure is a diagonal sub-surface strip structure.

5. The semiconductor device as recited in Claim 1 wherein said sub-surface structure is an axial sub-surface strip structure.

6. The semiconductor device as recited in Claim 1 wherein each conductive sub-surface region has an N-type doping.

7. The semiconductor device as recited in Claim 1 wherein each conductive sub-surface region has a P-type doping.

8. The semiconductor device as recited in Claim 1 wherein each conductive sub-surface region has a strip shape.

9. The semiconductor device as recited in Claim 1 wherein said metal structure has a metal wire shape.

10. The semiconductor device as recited in Claim 1 further comprising a plurality of second conductive sub-surface regions of said first conductivity each formed under each portion of said metal structure that overlaps said sub-surface structure, wherein each second conductive sub-surface region has a continuous sub-surface layer shape.

11. A semiconductor device having a surface, comprising:

a first plurality of conductive sub-surface regions of a first conductivity each formed beneath said surface, wherein said first plurality of conductive sub-surface regions form a first sub-surface structure for routing a body-bias voltage;

a second plurality of conductive sub-surface regions of said first conductivity each formed beneath said surface, wherein said second plurality of conductive sub-surface regions form a second sub-surface structure for routing said body-bias voltage;

an isolation structure formed between said first sub-surface structure and said second sub-surface structure such that said isolation structure creates a gap between said first sub-surface structure and said second sub-surface structure; and

at least one metal structure formed above said surface, wherein said metal structure spans said gap and is coupled to said first sub-surface structure and said second sub-surface structure via a plurality of tap contacts.

12. The semiconductor device as recited in Claim 11 wherein said first sub-surface structure is a first diagonal sub-surface mesh structure, and wherein said second sub-surface structure is a second diagonal sub-surface mesh structure.

13. The semiconductor device as recited in Claim 11 wherein said first sub-surface structure is a first axial sub-surface mesh structure, and wherein said second sub-surface structure is a second axial sub-surface mesh structure.

14. The semiconductor device as recited in Claim 11 wherein said first sub-surface structure is a first diagonal sub-surface strip structure, and wherein said second sub-surface structure is a second diagonal sub-surface strip structure.

15. The semiconductor device as recited in Claim 11 wherein said first sub-surface structure is a first axial sub-surface strip structure, and wherein said second sub-surface structure is a second axial sub-surface strip structure.

16. The semiconductor device as recited in Claim 11 wherein each conductive sub-surface region has an N-type doping.

17. The semiconductor device as recited in Claim 11 wherein each conductive sub-surface region has a P-type doping.

18. The semiconductor device as recited in Claim 11 wherein each conductive sub-surface region has a strip shape.

19. The semiconductor device as recited in Claim 11 wherein said metal structure has a metal wire shape.

20. The semiconductor device as recited in Claim 11 further comprising a plurality of second conductive sub-surface regions of said first conductivity each formed under each portion of said metal structure that overlaps said first and second

sub-surface structures, wherein each second conductive sub-surface region has a continuous sub-surface layer shape.

21. A semiconductor device having a surface, comprising:

a plurality of conductive sub-surface regions of a first conductivity each formed beneath said surface, wherein said conductive sub-surface regions form a sub-surface structure for routing a body-bias voltage, wherein said sub-surface structure has a perimeter;

an isolation structure formed within said perimeter of said sub-surface structure such that said isolation structure creates a gap in said sub-surface structure; and

at least one structure that spans said gap and is coupled to said sub-surface structure.

22. The semiconductor device as recited in Claim 21 wherein said sub-surface structure is a diagonal sub-surface mesh structure.

23. The semiconductor device as recited in Claim 21 wherein said sub-surface structure is an axial sub-surface mesh structure.

24. The semiconductor device as recited in Claim 21 wherein said sub-surface structure is a diagonal sub-surface strip structure.

25. The semiconductor device as recited in Claim 21 wherein said sub-surface structure is an axial sub-surface strip structure.

26. The semiconductor device as recited in Claim 21 wherein each conductive sub-surface region has an N-type doping.

27. The semiconductor device as recited in Claim 21 wherein each conductive sub-surface region has a P-type doping.

28. The semiconductor device as recited in Claim 21 wherein each conductive sub-surface region has a strip shape.

29. The semiconductor device as recited in Claim 21 wherein said structure is a polysilicon wire.

30. The semiconductor device as recited in Claim 21 wherein said structure is a diffusion wire.

31. The semiconductor device as recited in Claim 21 wherein said structure is a silicide wire.

32. The semiconductor device as recited in Claim 21 further comprising a plurality of second conductive sub-surface regions of said first conductivity each

formed under each portion of said structure that overlaps said sub-surface structure, wherein each second conductive sub-surface region has a continuous sub-surface layer shape.

33. The semiconductor device as recited in Claim 21 wherein said isolation structure divides said sub-surface structure into a first portion and a second portion.